



Application Note - Interpoint

Crane Aerospace & Electronics Power Solutions



Inhibit and Synchronization



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APPLICATION NOTE

Although the concepts stated are universal, this application note was written specifically for Interpoint products.

This application note describes the use and interface of the inhibit and synchronization (sync) terminals of Interpoint power converters. The inhibit function allows shutdown of the power converter without interrupting the connection to the input power bus. The sync function allows the power converter to be synchronized to an external clock or other devices.

INHIBIT

Interpoint power converters with inhibit functions are listed in Tables 1 and 2. The power supply is inhibited (shutdown) when the inhibit terminal is pulled low. An open collector transistor is the recommended interface, as shown in Figure 1.

The power converters of Table 1 are push-pull forward devices with the exception of the MSR Series, which is a single-ended flyback device. On all converters, the inhibit circuit is referenced to the input return line and the typical interface circuit is shown in Figure 1. The inhibit, when pulled low, disables the input MOSFET drive circuit and resets the soft start circuitry. An internal series diode allows the inhibit terminals of multiple devices to be connected together for operation from a single open collector external transistor. Figure 1 shows an open collector external transistor with the base circuit configured for TTL input levels. When the base is pulled high, the power converter is disabled due to the collector pulling the diode cathode low. An external pull up resistor is optional. A

resistor value of approximately 50K can be used where single or multiple power converters are involved.

In some applications, it may be necessary to reference the inhibit command to the output side of the power converter, which may be isolated from the input. To maintain isolation, an opto isolator is recommended as shown in Figure 2. The common emitter configuration of the open base photo transistor can be replaced with a photo diode or the faster two transistor configuration of Figure 3, where faster recovery from inhibit is required. The selection of the opto couplers and detail design is left to the user.

Table 2 showcases Interpoint's fully qualified products. Most of these products employ a single-ended forward

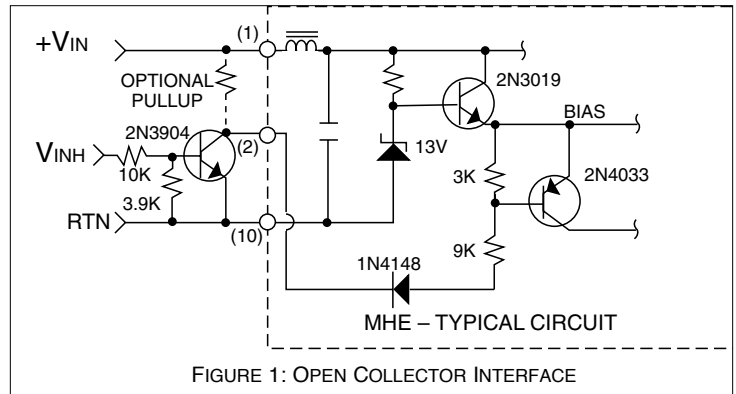


FIGURE 1: OPEN COLLECTOR INTERFACE

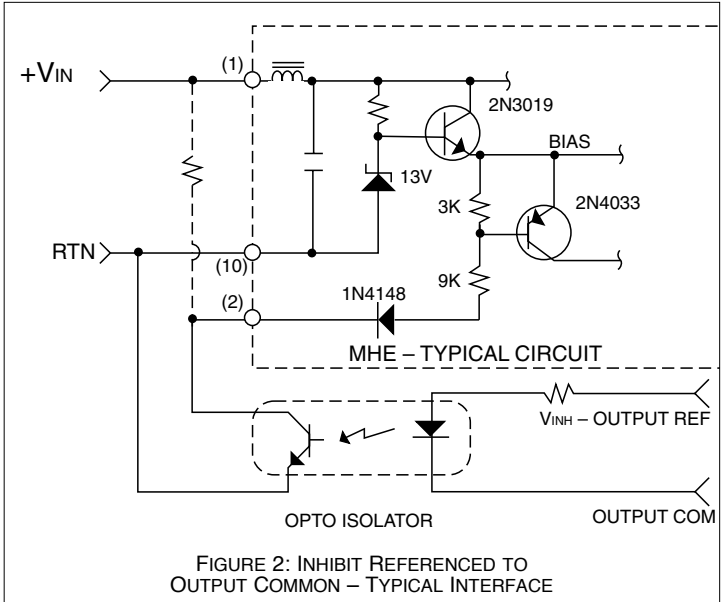
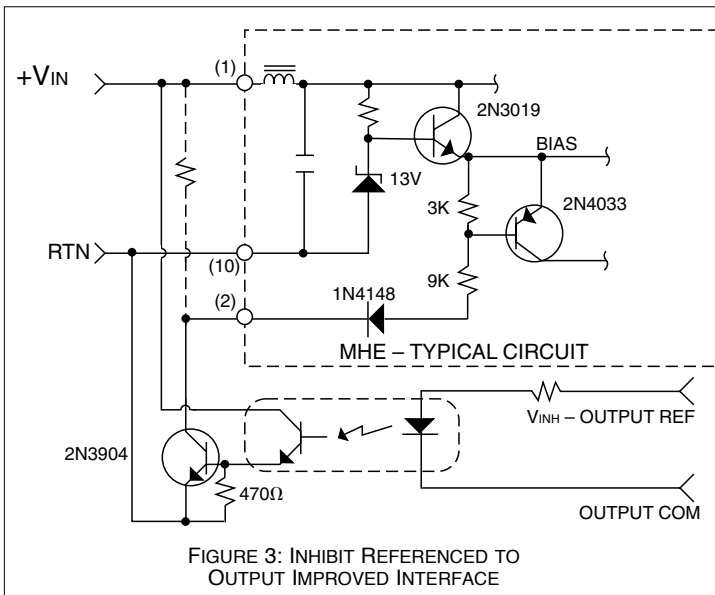
TABLE 1: INHIBIT CHARACTERISTICS OF FIRST GENERATION DC/DC CONVERTERS			
Model	Inhibit Location	Open Circuit Voltage	Inhibit Pin Current
MHE	Input – Pin 2	< 13 Volts	< 2.0 mA
MLP	Input – Pin 2	< 13 Volts	< 2.0 mA
MTO	Input – Pin 8	< 13 Volts	< 2.0 mA
MTW Single	Input – Pin 2	< 13 Volts	< 3.0 mA
MTW Dual	Input – Pin 8	< 13 Volts	< 3.0 mA
MFW	Input – Pin 4	4.5V to 5.5V	< 1.0 mA
MSR Single & Dual	Input – Pin 15	$V_{LINE} - 0.7$ Volts	< 1.0 mA
MSR Triple	Input – Pin 15	< 13 Volts at 28 V_{LINE} < 20 Volts at 50 V_{LINE}	< 2.0 mA
MHL	Input – Pin 8	< 9.5 Volts	< 2.5 mA

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design. The exceptions are the MSA and MCH Series which are single-ended flybacks and the FM704A which is a filter and transient suppressor. Where very fast turnoff is required, such as in a nuclear event application, these devices are recommended over the converters shown in Table 1. A typical inhibit circuit and interface is shown in Figure 4. Here, the inhibit signal shuts off the internal bias supply, resulting in fast turnoff of the power switch. All of the products have inhibit terminals referenced to input common. Additionally, the MFL and MOR Series have a second inhibit terminal on the secondary side referenced to output common. The open collector transistor interface of Figure 4 can be used in all cases where isolation is not required, including the MFL and MOR output referenced inhibits. Where the inhibit circuit requires isolation, the faster common collector opto isolator configuration of Figure 3 is recommended.

The inhibit terminals of the power converters in Table 2 do not incorporate a series diode. In cases of multiple usage where several inhibit terminals are connected together and operated by a single open collector, the diode must be added externally. A diode anode is connected to each power converter inhibit terminal with the cathodes connected together and to the open collector interface transistor. Interpoint recommends fast low level diodes such as type 1N4148.



SYNCHRONIZATION

Table 3 lists Interpoint power converters with a sync function. TTL levels are recommended, but slightly larger levels may be used without a problem. However, the maximum positive level should not exceed 5.5 volts. The ideal sync input signal is a 50% duty cycle square wave with rise and fall times less than 100 nanoseconds and low and high levels of <0.8 volts and 4.5 to 5.2 volts, respectively. A positive going pulse is also an effective sync signal. In this case, the duty cycle should be >4% and rise and fall times <20 nanoseconds for the minimum duty cycle. An interface driver with $Z_o < 50$ ohms is recommended.

The sync and clock circuit for the MFL power converter is shown in Figure 5. Sync occurs on the positive edge of the input wave form at terminal 6. This causes the positive terminal of the LM319 to be pulled below its negative input, switching the output negative and resetting the exponential timing voltage on capacitor C3. Early termination of each clock cycle then causes synchronization. Each of the power converters in Table 3 includes a sync input and clock circuit similar to that in Figure 5. The MFL and MOR Series, however, are the only models with a sync output pulse. This short duty cycle pulse, referenced to the input return, can be used as a source to sync other power converters. A low impedance interface circuit with a totem pole or complementary follower type output should be used as a buffer in this application.

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Model	Inhibit Location	Open Circuit Voltage	Inhibit Pin Current
MCH	Input – Pin 7	< 12.0 Volts	< 1 mA
MSA	Input – Pin 5	< 11.0 Volts	< 4.0 mA
MHF	Input – Pin 1	< 11.0 Volts	< 2.5 mA
MHF+ Single & Dual	Input – Pin 1	< 11.0 Volts	< 3.0 mA
MHF+ Triple	Input – Pin 1	< 10.0 Volts	< 6.0 mA
MHV Single & Dual	Input – Pin 2	< 12.0 Volts	< 9.0 mA
MHV Triple	Input – Pin 8	< 12.0 Volts	< 9.0 mA
MHD Single & Dual	Input – Pin 2	< 11.5 Volts	< 5.5 mA at 28 V _{LINE} < 10.0 mA at 50 V _{LINE}
MTR Single & Dual	Input – Pin 2	< 11.5 Volts	< 5.5 mA at 28 V _{LINE} < 10.0 mA at 50 V _{LINE}
MTR Triple	Input – Pin 8	< 11.5 Volts	< 3.0mA at 28 V _{LINE} < 5.0 mA at 50 V _{LINE}
MFL	Input – Pin 4	< 11.5 Volts	< 6.0 mA
MOR	Output – Pin 12	< 8.0 Volts	< 7.0 mA
	Input – Pin 4	< 13.0 Volts	< 1.0 mA
	Output – Pin 12	< 8.0 Volts	< 1.0 mA
FM – 704A	Input – Pin 6	< 5.0 Volts	< 1.0 mA
MSS	Input – Pin 8	< 14.0 Volts	< 6.0 mA

Note: Refer to individual data sheets for additional information.

The sync input of all devices of Table 3 is referenced to the input power return. Applications where the sync signal source is referenced to the output common or other ground require an isolated interface circuit. This usually involves a pulse transformer as shown in Figure 6. Here, a low impedance complementary output buffer drives the pulse transformer. A capacitor in series with the primary removes the DC. The low impedance buffer allows multiple power converter sync inputs to be driven in parallel. The pulse transformer secondary turns can be altered to adjust the sync pulse amplitude as required for a particular application. If the pulse transformer is driven directly without the series capacitor, care must be taken to ensure that the core flux is reset to zero on a cycle by cycle basis to avoid core saturation.

Where multiple power converters are used with their inputs paralleled and sync inputs connected to a common pulse driver, care must be taken to ensure that unwanted noise signals, due to ground loops, do not appear as unwanted sync inputs. When a sync terminal is referenced to the power converter input return, any noise between this return and the sync driver common will appear as a spurious sync input. This can cause jitter and low frequency components

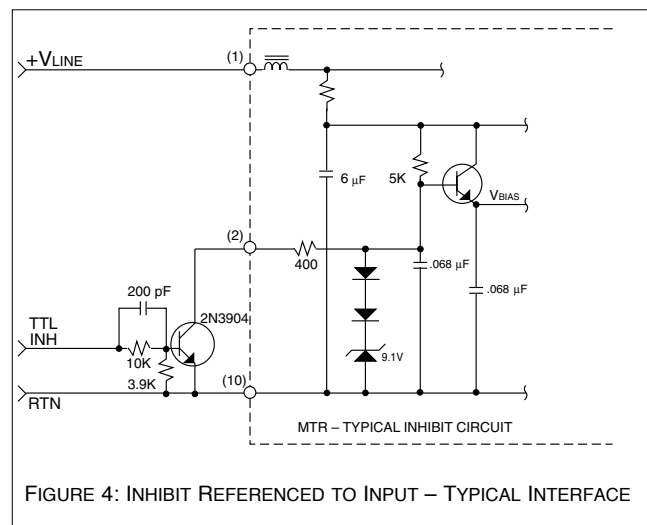


FIGURE 4: INHIBIT REFERENCED TO INPUT – TYPICAL INTERFACE

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TABLE 3: SYNC INPUT/OUTPUT CHARACTERISTICS					
SYNC INPUT					
Model	Sync. Location	Freq. Range	Levels	Duty Cycle	
				Square Wave	Pulse
MFL	Input – Pin 6	525 to 675 kHz	↑ 4.5 to 5.2V High < 0.8V Low ↓	40% to 60%	> 4%
MOR	Input – Pin 6	525 to 625 kHz		40% to 60%	> 4%
MFLHP	Input – Pin 6	525 to 675 kHz		40% to 60%	> 4%
MTR* Single & Dual	Input – Pin 9	500 to 675 kHz		40% to 60%	> 4%
MTR* Triple	Input – Pin 9	500 to 675 kHz		40% to 60%	> 4%
MHD* Single & Dual	Input – Pin 9	500 to 675 kHz		40% to 60%	> 4%
MHF+* Single & Dual	Input – Pin 5	500 to 600 kHz		40% to 60%	> 4%
MHF+ Triple	Input – Pin 7	400 to 600 kHz	↓ 4.5 to 10.0V High < 0.8V Low	40% to 60%	> 4%
MHV Single & Dual	Input – Pin 9	500 to 700 kHz		40% to 60%	> 4%
MHV Triple	Input – Pin 9	600 to 700 kHz		40% to 60%	> 4%
Rise & Fall Time				< 100 nsec.	< 20 nsec.
SYNC OUTPUT					
MFL* – All	Input – Pin 5	575 kHz typ.	9.0 to 10.0V Hi < 0.8V Low	–	5% typ.
MOR	Input – Pin 5	575 kHz typ.	9.0 to 10.0V Hi < 0.8V Low	–	5% typ.

*If the sync input terminal is not used, it must be grounded to input common
 Note: Refer to individual data sheets for more detailed information

in the input and output spectral noise. If this is important to the user, eliminate the ground loops or use pulse transformers to decouple the noise. Use pulse transformers or a multiple secondary pulse transformer on one or more sync inputs as required. Figure 8 shows an example where three power converter inputs are paralleled and synchronized from the same pulse driver. The sync input of converter #1 is driven directly from the sync pulse driver because its return is close to the #1 power converter return. Power converters #2 and #3 share a common ground loop between their returns and the driver return. A dual secondary pulse transformer is used to decouple the sync terminals from noise in the ground loop.

INHIBIT AND SYNCHRONIZATION WITH EMI FILTER
 Where switching power supplies are used with power line EMI filters, extra care must be exercised in locating the external ground returns for the inhibit and/or synchronization functions. Referencing these ground returns to anything other than the power converter 28 volt input return may cause catastrophic damage to the power converter.

The power line filter usually incorporates a balun as part of the common mode noise filter (refer to Figure 8). One winding of the balun is in series with the filter return line. If the return for the sync generator or the inhibit pull down switch is terminated at the input return side of the filter, any noise developed across this balun winding will appear

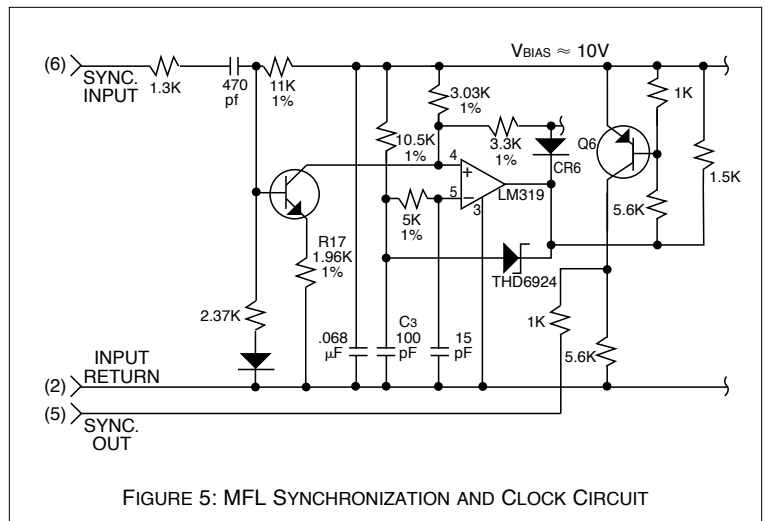


FIGURE 5: MFL SYNCHRONIZATION AND CLOCK CIRCUIT

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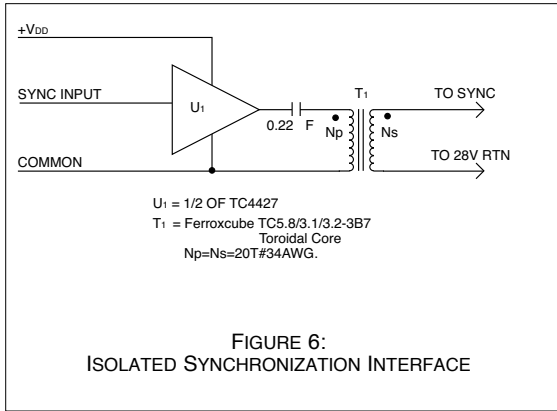


FIGURE 6:
ISOLATED SYNCHRONIZATION INTERFACE

as an input in series with either of these functions. The voltage developed across this winding will

The inhibit is controlled from an opto-isolator whose output transistor is connected to the input return of the power converters. Isolation diodes are used to allow the inhibit terminals to be controlled from a single source. It is assumed that the power converters are located next to each other so that any effective series resistance or series

consist of high frequency noise components with a peak-to-peak amplitude of several volts. This is sufficient to disrupt the pulse width modulator (PWM), resulting in saturation of the power transformer, catastrophic damage to the power train components, and damage to the FET power switch.

Figure 8 is an example where two power converters are connected to a common filter. Both the inhibit and sync functions are in use. A pulse transformer isolates the sync input from the ground loop containing the balun in the line filter. Without the isolation, voltage across the return line balun winding would be in series with the sync generator.

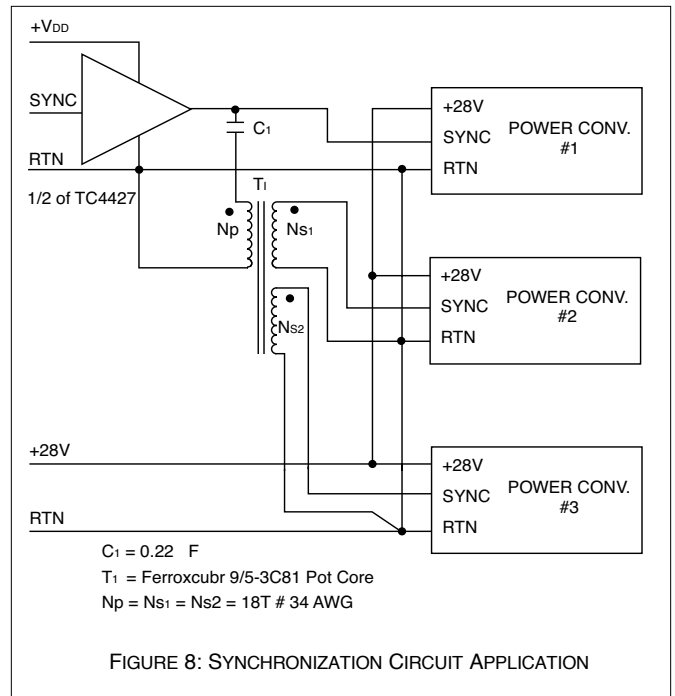


FIGURE 8: SYNCHRONIZATION CIRCUIT APPLICATION

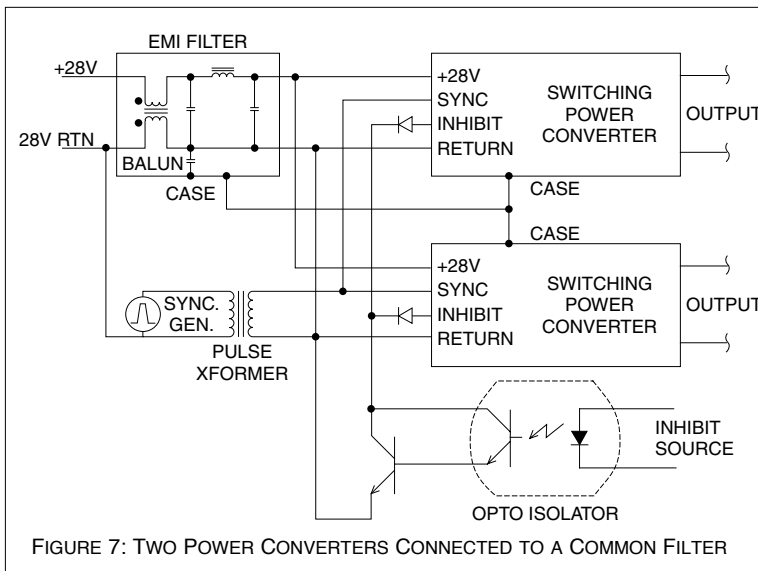


FIGURE 7: TWO POWER CONVERTERS CONNECTED TO A COMMON FILTER

inductance associated with the common ground connection between the two is negligible.